WHAT IS CLAIMED:

1. A circuit, comprising:

a matched filter circuit coupled to receive a plurality signals within a time slot, the plurality of signals including a sequence of predetermined signals interposed within a plurality of data signals, the matched filter circuit producing an output signal in response to the data signals; and

a decode circuit coupled to receive the output signal, the output signal including a first data symbol and a transform of a second data symbol, the decode circuit producing a decoded first data symbol and a decoded second data symbol.

2. A circuit as in claim 1, wherein the decode circuit produces each of the decoded first data symbol and the decoded second data symbol in response to the first data symbol and the transform of the second data symbol.

3. A circuit as in claim 2, wherein the transform of the second data symbol is a complex conjugate of the second data symbol.

4. A circuit as in claim 1, wherein the predetermined signals comprise a midamble.

5. A circuit as in claim 1, wherein the matched filter circuit further comprises a plurality of fingers coupled to receive the plurality of signals, and wherein each finger corresponds to a respective path of the plurality of signals, each finger producing a respective output signal.

6. A circuit as in claim 5, wherein the respective output signal of each finger of the plurality of fingers comprises plural output signals, and wherein each of the plural output signals corresponds to a respective shift of a code of the predetermined signals.

7. A circuit as in claim 6, wherein said each respective shift of a code of the predetermined signals is a respective shifted sample of a code sequence.

8. A circuit as in claim 6, further comprising:

a plurality of decode circuits, each decode circuit coupled to receive the plural output signals from a respective finger, each decode circuit arranged to produce a respective first decoded symbol and a respective second decoded symbol; and

a joint detector circuit coupled to receive the respective first decoded symbol and the respective second decoded symbol from each respective decode circuit, the joint detector circuit combining the respective first decoded symbol and the respective second decoded symbol from each said finger corresponding to each said respective code.

9. A circuit as in claim 8, wherein the joint detector attenuates interference by parallel interference cancellation.

10. A circuit as in claim 8, wherein the joint detector attenuates interference by zero forcing interference cancellation.

11. A circuit as in claim 8, wherein the joint detector attenuates interference by minimum mean squared error interference cancellation.

12. A circuit as in claim 1, wherein the predetermined signals within each time slot correspond a respective user, and wherein the predetermined signals corresponding to each user are encoded with a respective shift of a code sequence.

13. A circuit, comprising:

a matched filter circuit having a plurality of fingers and coupled to receive a respective plurality signals, the plurality of signals including a sequence of predetermined signals and a plurality of data signals having a spreading factor of one, the matched filter circuit producing an output signal in response to the data signals;

a decode circuit coupled to receive the output signal, the output signal including a first data symbol and a transform of a second data symbol, the decode circuit producing a decoded first data symbol and a decoded second data symbol; and

an equalizer circuit coupled to receive the decoded first data symbol and the decoded second data symbol, the equalizer circuit producing an output signal corresponding to a predetermined code.

14. A circuit as in claim 13, wherein each finger corresponds to a respective path of the plurality of signals, and wherein each finger produces a respective output signal.

15. A circuit as in claim 13, wherein the decode circuit produces each of the decoded first data symbol and the decoded second data symbol in response to the first data symbol and the transform of the second data symbol.

16. A circuit as in claim 15, wherein the transform of the second data symbol is a complex conjugate of the second data symbol.

17. A circuit as in claim 13, wherein the decode circuit is further coupled to receive a transform of the first data symbol and the second data symbol.

18. A circuit as in claim 13, wherein the equalizer circuit attenuates interference by zero forcing interference cancellation.

19. A circuit as in claim 13, wherein the equalizer circuit attenuates interference by minimum mean squared error interference cancellation.

20. A circuit, comprising:

a matched filter circuit coupled to receive a first data symbol and a transform of a second data symbol, the matched filter circuit producing an output signal; and

a joint detector circuit coupled to receive each respective output signal from the plurality of rake receiver circuits, the joint detector circuit producing an output signal corresponding to a predetermined code.

21. A circuit as in claim 20, wherein the predetermined code corresponds to a mobile receiver.

22. A circuit as in claim 20, wherein the predetermined code is a subset of a code sequence corresponding to a plurality of mobile receivers.

23. A circuit as in claim 20, wherein the joint detector circuit further comprises a decoding circuit.

24. A circuit as in claim 20, wherein the decode circuit is further coupled to receive a transform of the first data symbol and the second data symbol.

25. A circuit as in claim 20, wherein the equalizer circuit attenuates interference by zero forcing interference cancellation.

26. A circuit as in claim 20, wherein the equalizer circuit attenuates interference by minimum mean squared error interference cancellation.

27. A circuit as in claim 20, wherein the equalizer circuit attenuates interference by parallel interference cancellation.

28. A circuit, comprising an encoder circuit coupled to receive a plurality of first and second symbols, the encoder circuit producing the plurality of first symbols at a first output terminal and a

transform of the plurality of second symbols at a second output terminal within a time slot, the encoder circuit producing a sequence of predetermined signals interposed within the plurality of first symbols.

29. A circuit as in claim 28, further coupled to receive a control signal, the encoder circuit producing the plurality of first symbols at the first output terminal and the transform of the plurality of second symbols at the second output terminal in response to a first value of the control signal, the encoder circuit producing the plurality of first symbols at the first output terminal and not producing the transform of the plurality of second symbols at the second output terminal in response to a second value of the control signal.

30. A circuit as in claim 28, further comprising a diversity control circuit coupled to receive a first input signal, the diversity control circuit producing the control signal corresponding to the first input signal.

31. A circuit as in claim 28, wherein the first input signal corresponds to a Doppler frequency.

32. A circuit as in claim 28, wherein the diversity control circuit is further coupled to receive a second input signal corresponding to a handoff signal.

33. A circuit as in claim 28, wherein the first input signal corresponds to a handoff signal.

34. A circuit as in claim 28, wherein the encoder circuit produces a midamble after the first symbol and before the second symbol.

35. A circuit as in claim 28, wherein the sequence of predetermined signals comprises a code sequence, and wherein a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal.

36. A circuit, comprising a filter circuit coupled to receive a sequence of predetermined signals from a first and a second remote antenna, wherein the sequence of predetermined signals comprises a code sequence, and wherein a first shift of the code sequence corresponds to the first remote antenna and a second shift of the code sequence corresponds to the second remote antenna, the filter circuit producing an output signal in response to the data signals.

37. A circuit as in claim 36, wherein the predetermined signals comprise a midamble.

38. A circuit as in claim 36, wherein said each respective shift of a code of the predetermined signals is a respective shifted sample of a code sequence.

39. A circuit, comprising an encoder circuit coupled to receive a plurality of symbols, the encoder circuit producing the plurality of symbols and a sequence of predetermined signals at a first and a second output terminal, wherein the sequence of predetermined signals comprises a code sequence, and wherein a first shift of the code sequence corresponds to the first output terminal and a second shift of the code sequence corresponds to the second output terminal.